WHAT IS CLAIMED IS:

1. A method of forming a conductive pattern of a semiconductor device, comprising:

forming a conductive layer on a substrate such that the conductive layer protrudes above an upper surface of the substrate;

forming a polishing protection layer on the substrate, including over the conductive layer, whereby the polishing protection layer presents a step between a portion of the polishing protection layer lying directly over the substrate and a portion of the polishing layer lying over the conductive layer;

forming a step compensation layer on the polishing protection layer that reduces the step presented by the polishing protection layer;

removing portions of the step compensation layer and the polishing protection layer to expose the conductive layer; and

etching away part of the exposed conductive layer to form a conductive pattern on the substrate.

2. The method of claim 1, wherein said forming of the polishing protection layer comprises forming one of a carbon, oxide and nitride layer on the substrate, including over the conductive layer.

3. The method of claim 2, wherein said forming of the polishing protection layer comprises forming one of a silicon nitride, aluminum oxide, diamond phase carbon, aluminum nitride and boron nitride layer on the substrate, including over the conductive layer.

4. The method of claim 1, wherein said forming of the step compensation layer comprises forming a layer of reflowable material on the polishing protection layer.

5. The method of claim 4, wherein the material is selected from the group consisting of flowable oxide, boro-phosphor silicate glass, spin on glass, photoresist, undoped silicate glass, phosphor silicate glass, boro silicate glass and tetra ethyl ortho silicate.

6. The method of claim 4, wherein the step compensation layer is formed by a chemical vapor deposition process or a spin coating process.

7. The method of claim 1, wherein said removing portions of the step compensation layer and the polishing protection layer comprises removing only some of the step compensation layer and the polishing protection layer using a first planarization process.

8. The method of claim 7, wherein the first planarization process is an etch-back process.

9. The method of claim 7, wherein said etching away part of the exposed conductive layer to form a conductive pattern comprises etching the step compensation layer, the polishing protection layer and the conductive layer using a second planarization process.

10. The method of claim 9, wherein the second planarization process is a chemical mechanical polishing process.

11. The method of claim 9, further comprising subsequently removing a remaining portion of the polishing protection layer from around the conductive pattern.

12. The method of claim 11, wherein said remaining portion of the polishing protection layer is removed using an etching solution including phosphoric acid.

13. A method of manufacturing a non-volatile semiconductor memory device comprising:

forming a structure including a floating gate on a substrate;

forming a conductive layer on the substrate including over the structure;

forming a polishing protection layer on the conductive layer, whereby the polishing protection layer presents a step between a portion of the polishing protection layer lying directly over the substrate and a portion of the polishing layer lying over the conductive layer;

forming a step compensation layer on the polishing protection layer that reduces the step presented by the polishing protection layer;

removing portions of the step compensation layer and the polishing protection layer to expose the conductive layer; and

etching away part of the exposed conductive layer to form a conductive pattern on the substrate;

forming an oxide layer on the conductive pattern; and

etching the conductive pattern using the oxide layer as an etching mask to form a control gate adjacent the floating gate.

14. The method of claim 13, wherein said removing portions of the step compensation layer and the polishing protection layer comprises removing only some of the step compensation layer and the polishing protection layer using a first planarization process.

15. The method of claim 14, wherein the first planarization process is an etch-back process.

16. The method of claim 13, wherein said etching away part of the exposed conductive layer to form a conductive pattern comprises etching the step compensation layer, the polishing protection layer and the conductive layer using a second planarization process.

17. The method of claim 16, wherein the second planarization process is a chemical mechanical polishing process.

18. The method of claim 13, wherein said forming the oxide layer comprises oxidizing the conductive pattern.

19. The method of claim 13, further comprising removing a residual portion of the polishing protection layer from around the conductive pattern after the control gate is formed.

20. The method of claim 19, wherein the residual portion of the polishing protection layer is removed using an etching solution including phosphoric acid.